## REMARKS

### Present Status of the Application

The Advisory Action rejected all presently-pending claims 1-22 because Examiner assert that Applicant's argument has been addressed in the rejection. Additionally, Examiner asserts that electrodes 13', 17' and 19 recited in U.S. Patent No. 5,734,449 are very similar to Applicant's figure 2H. Applicants have added a new claim (claim 22) to more explicitly describe the present invention.

### Discussion of Office Action Rejections

The Office Action rejected claims 1-21 under 35 U.S.C. 103(a), as being unpatentable over Jang (U.S. Patent No. 5,734,449). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claim 1 recites the features as follows:

1. A pixel structure, comprising:

a scan line, disposed over a substrate;

a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;

a plurality of ***transparent capacitance electrodes***, disposed over the substrate, ***wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode***; and

a pixel electrode, disposed over the transparent capacitance electrodes and electrically connected to the active component,

wherein the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor.

***(Emphasis added).***

Claims 2-9 also recite the similar features.

Independent claim 10 recites the features as follows:

10. A manufacturing method, for a pixel structure, comprising:

sequentially forming an active component, a scan line and a data line over a substrate, wherein the active component is electrically connected to the scan line and the data line;

forming ***a plurality of transparent capacitance electrodes*** over the substrate, ***wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode formed above the first transparent capacitance electrode***; and

forming a pixel electrode over the transparent capacitance electrodes, wherein the pixel electrode is electrically connected to the active component, wherein the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor.

***(Emphasis added).***

Claims 11-19 also recite the similar features.

Independent claim 10 recites the features as follows:

20. A pixel structure, comprising:
a scan line, disposed over a substrate;
a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;

***a first transparent capacitance electrode***, disposed over the substrate;

a pixel electrode, disposed over the first transparent capacitance electrode and electrically connected to the active component and the first transparent capacitance electrode; and

***a second transparent capacitance electrode, disposed between the first transparent capacitance electrode and the pixel electrode, wherein a multilayer pixel storage capacitor is formed by the pixel electrode, the first transparent capacitance electrode and the second transparent capacitance electrode.***

***(Emphasis added).***

Claim 21 also recite the similar features.

Independent claim 22 recites the features as follows:

22. A pixel structure, comprising:

a scan line, disposed over a substrate;

a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component comprises a gate electrically connected to the scan line, a channel disposed over the gate and a source/drain disposed over the channel and electrically connected to the data line and the pixel electrode;

***a protection layer, disposed over the substrate for covering the gate of the active component***;

***a plurality of transparent capacitance electrodes***, disposed over the substrate, the transparent capacitance electrodes comprising at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode, ***wherein the first transparent capacitance electrode is disposed on the protection layer***; and

a pixel electrode, disposed over the transparent capacitance electrodes and electrically connected to the active component, ***wherein the pixel electrode is electrically connected to the first transparent capacitance electrode such that the transparent capacitance electrodes constitute a multilayer pixel storage capacitor***.

In re U.S. Patent No. 5,734,449 (Column 2, line 66 ~ Column 3, line 6), Jang discloses that " In the liquid crystal display apparatus of the present invention as shown in FIG. 3, ***lower storage electrode 13' and upper storage electrode 17' of storage capacitor part 100 which is concurrently formed with black matrix 13 of thin film transistor part 50 as material for cutting off light and being conductive***, are connected in parallel as shown in FIG. 4, so that the total capacitance increases with the same manufacture area as a conventional one". As discussed by Jang, Applicant finds that the lower electrode 13' and upper storage electrode 17' of storage capacitor part 100 is made of ***opaque materials***. In this way, aperture ratio of the LCD apparatus illustrated by Jang is decrease. The larger the area occupied by storage capacitor part 100, the lower the aperture ratio is. Additionally, Jang failed to teach or suggest that the lower electrode 13' and upper storage electrode 17' of storage capacitor part 100 can be made of transparent materials. Obviously, the concept of ***transparent capacitance electrode*** is "NOT" proposed by Jang to enhance aperture ratio of the LCD apparatus. Therefore, Applicant considers that Claims 1-21 are patently distinguished from US Patent No. 5,734,449.

In the claimed invention, the aperture ratio is not affected by the area occupied by the storage capacitor (i.e. area of transparent capacitance electrodes) even the transparent capacitance electrodes of the storage capacitor occupy almost region under the pixel electrode. Accordingly, flexibility of layout design can be improved by the present invention significantly.

In re Column 2, line 66 ~ Column 3, line 6 of U.S. Patent No. 5,734,449, Jang teaches away that the lower electrode 13' and upper storage electrode 17' can be formed of ITO or IZO. Additionally, there is no evidence provided by the Examiner to prove that the capacitor plate formed of ITO or IZO is obvious. Therefore, Applicant considers that the Examiner fails to establish Prima Facie Case of obviousness and Claims 1-21 are patentable over US Patent No. 5,734,449.

To more explicitly describe the present invention, Applicants have added claim 22 to emphasize the feature "***the first transparent capacitance electrode is disposed on the protection layer***". In other words, Applicants have emphasized that the first transparent capacitance electrode is located between two different layers. The content of claim 22 is fully support by the specification (see figures 2H and 3F). Specifically, the gate of the active component is covered by the protection layer while the first transparent capacitance electrode is disposed on the protection layer. However, in the US Patent No. 5,734,449, Jang fail to disclose the feature "***the first transparent capacitance electrode is disposed on the protection layer***". In contrast,

Jang discloses that the upper storage electrode 17' and the gate electrode 17 are formed simultaneously.

Jang not only fails to disclose the first transparent capacitance electrode and the second transparent capacitance electrode, but also fails to disclose the manufacturing process as claimed in claim 10. ***Specifically, the active component and the capacitance electrode are formed simultaneously in the US Patent No. 5,734,449, while the active component and the transparent capacitance electrode are formed by different steps.***

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 10, 20 and 22 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-9, 11-19 and 21 patently define over the prior art as well.

Customer No.: 31561
Application No.: 10/709,090
Docket No.:12029-US-PA

## CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date : April 6, 2006

Respectfully submitted,

Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw